23-24

MAULANA ABUL KALAM AZAD UNIVERSITY OF TECHNOLOGY, WEST BENGAL

Paper Code : BCAC101 Digital Electronics

UPID : 100[illegible]

Time Allotted : 3 Hours | Full Marks :70

The Figures in the margin indicate full marks.

Candidate are required to give their answers in their own words as far as practicable

Group-A (Very Short Answer Type Question)

1. Answer *any ten* of the following : [1 x 10 = 10]

(i) Dual of NAND function is_____

(ii) The half adder has _____ inputs and full adder has _____ inputs.

(iii) What is the indication of a short to ground in the output of a driving gate?

(iv) How is a J-K flip-flop made to toggle?

(v) Ripple counters are also called _____

(vi) Convert 128 to binary

(vii) The NAND gate can functions as a NOT gate if_____

(viii) Reduce the expression f=A[B+C'(AB+AC')']

(ix) What is the minimum number of two-input NAND gates used to perform the function of two input OR gate?

(x) _____ are the universal gates.

(xi) Full subtractor is used to perform subtraction of _____bits.

(xii) How many data select lines are required for selecting eight inputs?

Group-B (Short Answer Type Question)

Answer *any three* of the following : [5 x 3 = 15]

2. Represent a NAND gate as OR gate using De Morgan's law and explain. [5]
3. What is the difference between a half adder and a full adder? [5]
4. Explain the difference between decoder & demultiplexer [5]
5. What is toggling state & race condition? [5]

6. Explain the difference between PISO & PIPO. [5]

Group-C (Long Answer Type Question)

Answer *any three* of the following : [15 x 3 = 45]

7. (a) Explain the difference between sequential circuit & combinational circuit. [7]
   (b) Explain SR Flip-flop in detail. What is the disadvantage of it and how it can be eliminated? [8]
8. (a) Design a combination circuits for a half & full subtractor and explain it in detail. [10]
   (b) Explain the limitations of half subtractor over full subtractor. [5]
9. (a) Design a full adder using 3:8 decoder. [8]
   (b) Explain the difference between multiplexer & demultiplexer [7]
10. (a) With logic diagram and truth table explain the working JK Flip-flop. Also obtain its characteristic equation. [7]
    (b) How JK flip-flop is the refinement of RS flip-flop? [4]

    (c) Explain D- Flip-flop in detail. [4]
11. (a) What is multiplexer? Explain 4X1 multiplexer. [2+7]
    (b) Explain encoder with proper diagram, truth table, Boolean expression [6]

*** END OF PAPER ***